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High Current Density and Nonlinearity Combination of Selection Device Based on $TaO_x/TiO_2/TaO_x$ Structure for One Selector–One Resistor Arrays

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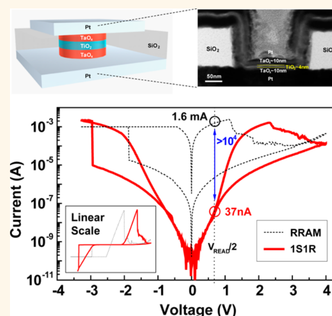
ABSTRACT We demonstrate a high-performance selection device by utilizing the concept of crested oxide barrier to suppress the sneak current in bipolar resistive memory arrays. Using a $TaO_x/TiO_2/TaO_x$ structure, high current density over 10^7 A cm^{-2} and excellent nonlinear characteristics up to 10^4 were successfully demonstrated. On the basis of the defect chemistry and SIMS depth profile result, we found that some Ta atoms gradually diffused into TiO_2 film, and consequently, the energy band of the TiO_2 film was symmetrically bent at the top and bottom TaO_x/TiO_2 interfaces and modified as a crested oxide barrier. Furthermore, the one selector–one resistor device exhibited significant suppression of the leakage current, indicating excellent selector characteristics.



KEYWORDS: resistance random access memory · selection device · nonlinearity · crested oxide barrier · one selector–one resistor

As conventional charge-based memories such as dynamic random access memory (DRAM), static random access memory (SRAM), and flash memory are approaching their scaling limits at the 1× technology node, various emerging research devices have been suggested for future high-density memory applications.[1–4] Among them, resistive random access memory (RRAM) has been one of the promising candidates to replace the aforementioned conventional memories due to RRAM's excellent scalability, simple structure, and fast switching speed.[5–12] On the basis of the bias polarity of its program and erase operations, RRAM can be classified into two types: unipolar[6,13–16] and bipolar.[10–12] The former can be programmed or erased at the same bias polarity, whereas the latter changes its resistance state by applying the opposite voltage polarity. Since bipolar RRAM has better device uniformity and endurance than a unipolar device,[17] it is better suited to realize a cross-point array with a $4F^2$ cell for high-density nonvolatile memory applications.

However, a cross-point array consisting of only RRAM can lead to a read failure due to the sneak path problem.[18,19] This problem can be maximized when accessed RRAM is in the high resistance state (HRS) whereas all neighboring devices are in the low resistance state (LRS) (see Figure S1, Supporting Information). In order to access the designated RRAM in a cross-point array, the read voltage should be applied between the corresponding word line and bit line, and consequently, the total read current can be much higher than the access current due to the sneak currents from undesignated neighboring cells. Therefore, the readout margin is significantly decreased as the array size increases, impeding the realization of high-density memory in the cross-point arrays. Although a transistor was proposed to overcome the sneak current issues,[20] it is hard to achieve the cell size of $4F^2$, thus eliminating the advantages of RRAM, such as excellent scalability.

To alleviate the misreading problem and achieve reliable high-density memory arrays, several groups have proposed various solutions in the form of devices such as complementary resistive switches[18] (CRS) and selection devices.[19,21–24] The CRS is composed of two antiserially connected bipolar RRAMs sharing a common electrode. It can effectively suppress the sneak current at

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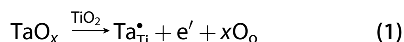
the low-voltage regime by turning off one of the RRAMs in the CRS. In the case of the selection device, several materials, such as a mixed ionic electronic conduction material,[21] an Ovonic threshold switching device,[22] a metal−insulator transition material,[19,23] and Schottky emission-based Ni/TiO_2/Ni stacks,[24] have been investigated for overcoming the sneak path problem. When these selection devices are connected with RRAM (defined as a 1S1R (one selector−one resistor) device), the sneak current paths can be suppressed due to their nonlinear *I*−*V* (current−voltage) characteristics (see Figure S1, Supporting Information). Moreover, the absence of a transistor can realize highly integrated memory architecture. However, to operate the nanoscale RRAM device, the maximum current density of the selection device should exceed 10^7 A cm^{-2}, since the reset current of nanoscale RRAM is typically over 10 μA.[25] In addition, the nonlinearity (defined as the current ratio between full-read voltage (V_{READ}) and half-read voltage ($V_{READ}/2$)) of the selection device is also an important factor for improving the readout margin in cross-point arrays. Likharev *et al.*[26] reported that the tunneling current through a crested energy barrier with the height peak in the middle could be dramatically increased compared to that through a uniform barrier height (Figure 1a and b). Since the highest part of a crested energy barrier is quickly reduced by an electric field, the tunneling current through such a barrier can change abruptly and, therefore, the degree of the nonlinearity can be significantly increased.

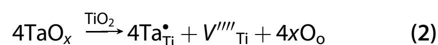
In this paper, a high-performance selection device using the concept of crested energy barrier is proposed to achieve both high current density and high nonlinearity for high-density bipolar RRAM applications. To make a crested energy barrier, we fabricated a selection device having a trilayer oxide structure and utilized defect chemistry during the device fabrication. Using a $TaO_x/TiO_2/TaO_x$ stack, sufficient current density over 10^7 A cm^{-2}, high nonlinearity up to 10^4, and excellent device immunity to read disturbances up to 10^{10} cycles were successfully demonstrated. This performance is the highest current density and nonlinearity combination compared to the previously reported selection devices such as VO_2,[23] TiO_2,[24] and poly-Si.[27] In addition, the characteristics of the 1S1R device were measured to confirm the suppression of leakage current, showing the leakage current in the 1S1R device was significantly reduced more than 4 orders of magnitude compared to the RRAM device.

RESULTS AND DISCUSSION

Figure 1c illustrates the experimental design of the selection device evaluated in this study. The device stack was composed of a TiO_2 layer sandwiched between TaO_x layers, and an inert Pt electrode was used for the top and bottom contacts. We choose a TiO_2 layer as a tunneling oxide material since it has been reported that the conductivity of TiO_2 film can be tuned by Nb or Ta doping.[28,29] Using these TaO_x and TiO_2 films, a crested oxide barrier can be formed as follows. During device fabrication, the Ta atoms in both the top and bottom TaO_x layers can diffuse into the TiO_2 layer by thermal energy. Since the ionic radius of Ta^{5+} is similar to that of Ti^{4+}, the Ti^{4+} in the TiO_2 film can be substituted by Ta^{5+} in the reactions[29] given in eqs 1 and 2.



$$TaO_x \xrightarrow{TiO_2} Ta^{\bullet}_{Ti} + e' + xO_o \quad (1)$$



$$4TaO_x \xrightarrow{TiO_2} 4Ta^{\bullet}_{Ti} + V''''_{Ti} + 4xO_o \quad (2)$$

where $Ta^{\bullet}_{Ti}$ is the substitution of Ti^{4+} with Ta^{5+}, O_o is the oxygen ion at the oxygen site, and V''''_{Ti} is a vacancy at the Ti site. Based on the above defect chemistry, the free electrons and defect sites were created, and consequently, the energy band of the TiO_2 film will be symmetrically bent at the top and bottom TaO_x/TiO_2 interfaces and modified as a crested oxide barrier. In addition, the TaO_x layer also acts as an internal resistor, which improves the device endurance and prevents a permanent breakdown.[30] To confirm the atomic profile and the device structure in the $TaO_x/TiO_2/TaO_x$ stack, a secondary ion mass spectroscopy (SIMS) depth profile and a cross-sectional image using transmission electron spectroscopy (TEM) are shown in Figure 1d and e, respectively. It is clearly observed that a 4-nm-thick TiO_2 layer was uniformly deposited and sandwiched between 10-nm-thick TaO_x layers in the 250 nm *via*-hole structure. Note that we deposited a conformal 4-nm-thick TiO_2 layer by atomic layer deposition (ALD) to serve as a tunneling barrier oxide in the selection device. According to the SIMS depth profile, the intensity of the Ta atom was minimized at the center of the TiO_2 layer and gradually increased at the top and bottom TaO_x/TiO_2 interfaces. These results imply that some amount of Ta atoms gradually diffused into the TiO_2 layer and formed the crested oxide barrier in the TiO_2 layer.

To compare the electrical characteristics of each oxide stack, Pt/TaO_x/Pt, Pt/TiO_2/Pt, and Pt/$TaO_x/TiO_2/TaO_x$/Pt (the selection device in this study) were fabricated. To minimize process variations, 10-nm-thick TaO_x in Pt/TaO_x/Pt (4-nm-thick TiO_2 in Pt/TiO_2/Pt) was deposited simultaneously with 10-nm-thick TaO_x (4-nm-thick TiO_2) deposition in a Pt/$TaO_x/TiO_2/TaO_x$/Pt stack. Figure 2a shows the typical *I*−*V* characteristics of each device. In the case of Pt/TiO_2/Pt, the device exhibited a highly insulating property with a barrier height of 1.5 eV, whereas the Pt/TaO_x/Pt device showed leaky behavior (Poole−Frenkel emission and ohmic conduction). On the basis of the Auger electron spectroscopy (AES) analysis, we infer that the insulating behavior in the TiO_2 was due to the negligible

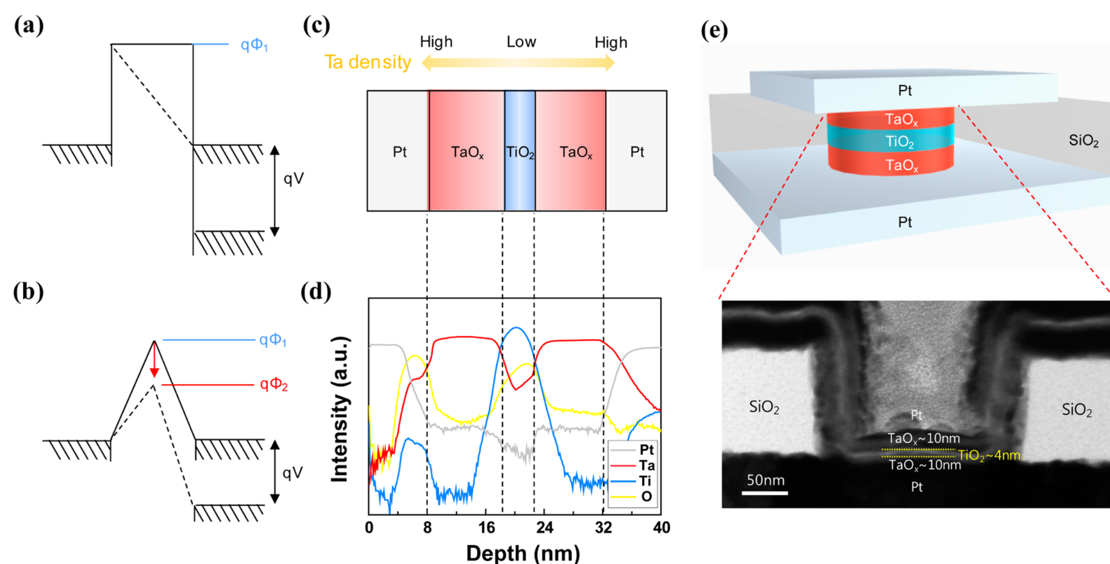


Figure 1. Schematic diagram of (a) typical uniform barrier and (b) ideal crested symmetric barrier. (c) Experimental design of the selection device and (d) SIMS depth profile of $Pt/TaO_x/TiO_2/TaO_x/Pt$ stack. (e) Schematic diagram of the device structure (top) and cross-sectional TEM image (bottom).

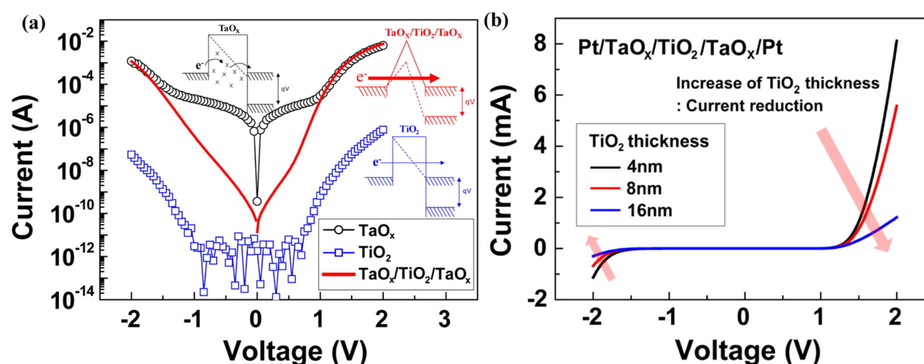


Figure 2. (a) Comparison of $I-V$ characteristics of the $Pt/TaO_x/Pt$, $Pt/TiO_2/Pt$, and $Pt/TaO_x/TiO_2/TaO_x/Pt$ stacks. The conceptual band diagrams for these structures were illustrated based on the electrical characteristics. Since the TaO_x film had many defects, we omitted Pt/TaO_x barriers in the $Pt/TaO_x/TiO_2/TaO_x/Pt$ stack. (b) Current dependence of the $Pt/TaO_x/TiO_2/TaO_x/Pt$ stack on TiO_2 thickness.

amount of defects, and the leaky property in the TaO_x layer originated from a high Ta defect concentration (detailed results are included in Figure S2, Supporting Information). On the other hand, by stacking TaO_x, TiO_2, and TaO_x, the current of the $Pt/TaO_x/TiO_2/TaO_x/Pt$ stack changed by more than 4 orders of magnitude between 0.7 and 1.4 V, exhibiting a highly nonlinear property with high current density. It is noteworthy that the current dramatically changed up to 1.2 V (−1.4 V) and eventually saturated due to the internal resistor in the TaO_x film.[30] In AES depth spectra, it is obvious that Ta atoms gradually diffused into the TiO_2 layer in the $Pt/TaO_x/TiO_2/TaO_x/Pt$ stack, which is well matched with the SIMS depth profile results in Figure 1c. Based on the electrical property, the conceptual band diagram of $Pt/TaO_x/Pt$, $Pt/TiO_2/Pt$, and $Pt/TaO_x/TiO_2/TaO_x/Pt$ stack is illustrated in Figure 2a.

In order to investigate the effect of TiO_2 thickness on the current level, we controlled the TiO_2 thickness in the $Pt/TaO_x/TiO_2/TaO_x/Pt$ stack, as shown in Figure 2b. As a result, all devices showed similar $I-V$ nonlinearity, but the current level decreased monotonically with increasing TiO_2 thickness. Since the conductivity of the $Pt/TaO_x/TiO_2/TaO_x/Pt$ stack is determined by TiO_2 thickness and Ta defect density, the electrons in the selection device with a thicker TiO_2 layer will have a hard time tunneling through the crested oxide barrier, resulting in current reduction. Note that although our selection device had a symmetric structure, the current behavior showed an asymmetric $I-V$ curve. Since Ta atoms were diffused into the TiO_2 film during the furnace annealing and ALD process, the defect density of the upper and lower sides of the TiO_2 film will not be the same. Therefore, the crested barrier will not be perfectly symmetric, resulting in asymmetric $I-V$ behavior in our device. By precisely controlling the tunneling oxide thickness and defect density, it might be possible to

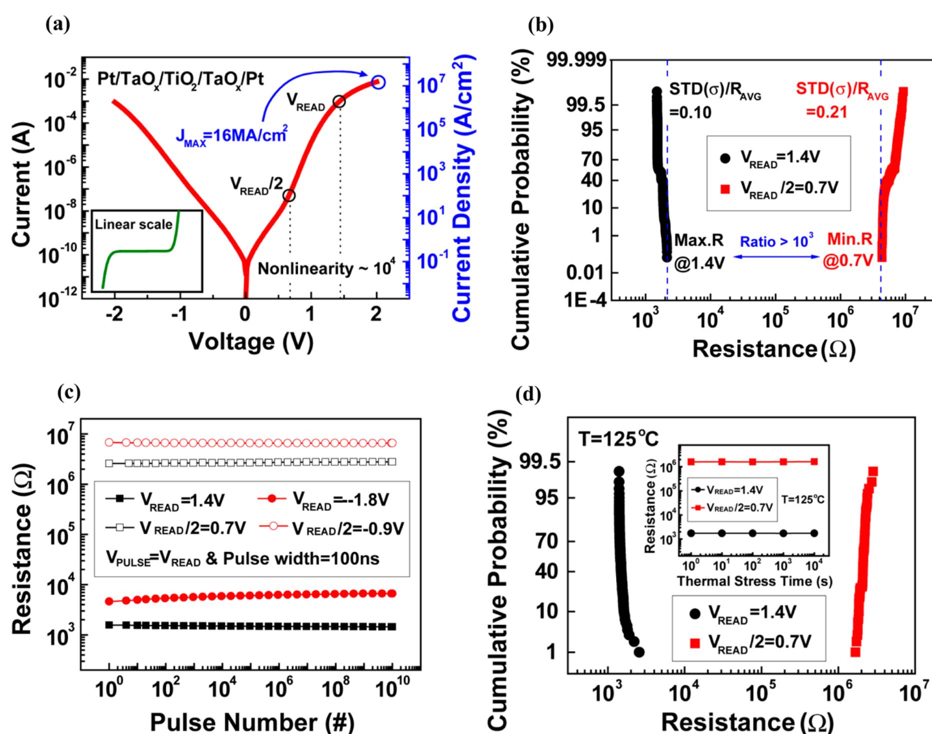


Figure 3. (a) Typical *I*−*V* characteristics of a Pt/TaO_x/TiO_2/TaO_x/Pt stack. The left axis corresponds to the current value, and the right axis represents the current density of the device. Inset shows the *I*−*V* curve of the device on a linear scale, indicating a highly nonlinear property. (b) Cumulative probability of resistance at V_{READ} and $V_{READ}/2$. (c) Pulse disturbance test of the device, demonstrating reliable operations. (d) Cumulative probability of resistance at V_{READ} and $V_{READ}/2$ at 125 °C to confirm the thermal operation of the device. Inset shows the result of the thermal stress test for up to 10^4 s at 125 °C.

regulate the tunneling current to meet the specifications for various RRAM operations.

Figure 3a represents typical *I*−*V* characteristics in a Pt/TaO_x/TiO_2/TaO_x/Pt stack on a semilog scale. We applied a voltage from 0 to 2 V (from 0 to −2 V for the negative region), and the direction of current flow was defined as top electrode (TE) to bottom electrode (BE). To perform read operation in the $n \times m$ cross-point array, for example, $V_{READ}/2$ and $-V_{READ}/2$ can be applied to the word line and bit line of the targeted cell, respectively. At this half-biased scheme, V_{READ} is effectively applied to the targeted cell, whereas $V_{READ}/2$ and $-V_{READ}/2$ are imposed to $(n + m - 2)$ cells sharing the targeted word line and bit line of the targeted cell, mainly contributing to the sneak current. Therefore, $V_{READ}/2$ and $-V_{READ}/2$ should be carefully selected to minimize the sneak current in the cross-point array. Herein, we assumed that V_{READ} and $V_{READ}/2$ correspond to 1.4 and 0.7 V, since the nonlinearity at these voltages shows the highest value in Figure 3a. The maximum current density was observed as 1.6×10^7 A cm^{-2} at 2 V, and the current at 1.4 and 0.7 V was 1.4 mA and 93 nA, respectively. The nonlinearity, which is an important factor for the readout margin, between V_{READ} and $V_{READ}/2$ was almost 10^4. The inset of Figure 3a shows *I*−*V* characteristics on a linear scale and accentuates the highly nonlinear property of the Pt/TaO_x/TiO_2/TaO_x/Pt stack, suggesting that the device is suitable for use in the selection device.

To evaluate the reliability of the device, a dc cycling test was performed, and the cumulative probability of the resistance is shown in Figure 3b. During 10^3 successive dc cycles, the device showed negligible degradation at V_{READ} and $V_{READ}/2$, indicating a highly reproducible nonlinear property of the Pt/TaO_x/TiO_2/TaO_x/Pt stack. For stable selection behavior in the 1S1R configuration, the device needs to exhibit an excellent disturbance property at V_{READ} and $V_{READ}/2$ without any breakdown or current degradation. We assigned V_{READ} and $V_{READ}/2$ to 1.4 V (−1.8 V) and 0.7 V (−0.9 V), respectively. By applying these pulses and read voltages with a 100 ns pulse width, we measure the resistance values during a pulse disturbance test as shown in Figure 3c. A stable nonlinear property was confirmed for up to 10^{10} cycles, demonstrating excellent device immunity to the read disturbance. Thermal stability is also important for reliable device operations. Figure 3d represents the cumulative probability of resistance at V_{READ} and $V_{READ}/2$ in the device during 100 dc cycles, which had substrate temperatures of 125 °C. A reproducible nonlinearity was observed at the elevated temperatures, suggesting stable thermal operation of the device. Furthermore, the device's robust resistance to thermal stress was also confirmed, as shown in the inset of Figure 3d. These results

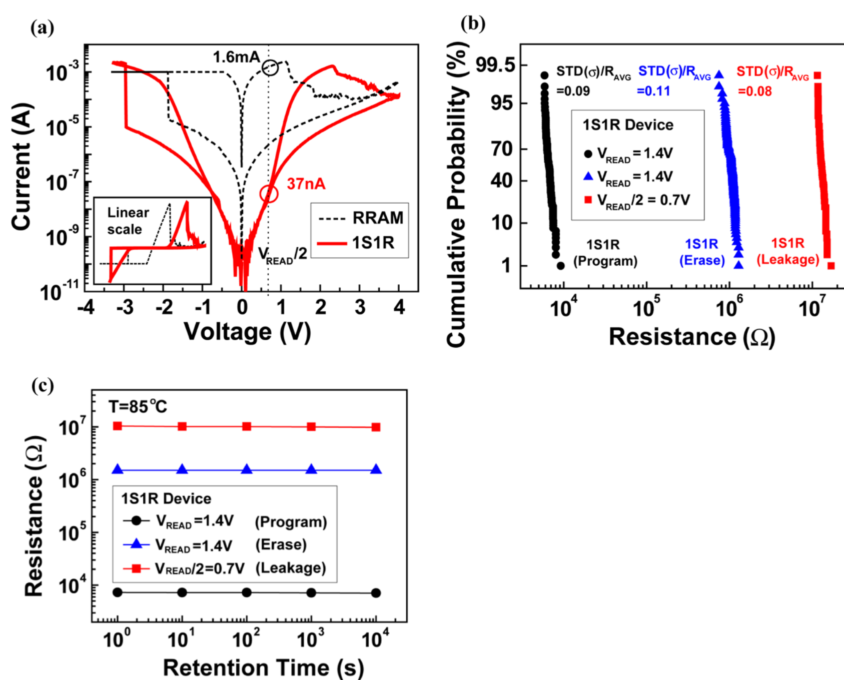


Figure 4. (a) Comparison of the leakage current between the 1S1R and RRAM, showing that the leakage current in the 1S1R was reduced by more than 4 orders of magnitude compared to RRAM. Inset shows the *I*−*V* characteristics of the 1S1R device and RRAM, accentuating the suppresstion of leakage current due to the excellent nonlinearity in the Pt/TaO_x/TiO_2/TaO_x/Pt stack. (b) Cumulative probability of resistance in the 1S1R at V_{READ} and V_{READ}/2. (c) Retention characteristics of the 1S1R device at 85 °C.

suggest that the Pt/TaO_x/TiO_2/TaO_x/Pt stack shows excellent reliability for the purpose of selection device applications.

To evaluate the 1S1R device feasibility in the cross-point array, we measured *I*−*V* characteristics and compared the leakage current of the 1S1R device with RRAM, as shown in Figure 4a. For the RRAM device, a Pt/Cu-doped HfO_2/Pt stack was fabricated. Details of fabricating Pt/Cu-doped HfO_2/Pt stacks have been described elsewhere.[31] Prior to the measurement of the 1S1R device, we had already confirmed that the fabricated RRAM exhibited stable resistive switching and retention characteristics at high temperature (see Figure S3, Supporting Information). Compared to the RRAM device, the leakage current of the 1S1R device is significantly reduced by more than 4 orders of magnitude at V_{READ}/2. Since the resistance of the selection device is much higher than RRAM's from −0.9 to 0.7 V, most of the applied voltage dropped at the selection device, thus suppressing the leakage current of the RRAM. In the set/reset operations in the 1S1R device, the applied voltage ($V < -0.9$ for set and $V > 0.7$ for reset) mainly dropped at the RRAM, and therefore, the RRAM changed its resistance state according to the bias polarity. Due to the excellent nonlinearity of the 1S1R device, the readout margin in the cross-point array was calculated to be dramatically improved compared to the RRAM device. Moreover, the maximum array size can be further increased if the current at V_{READ}/2 in the 1S1R device is reduced more (see Figures S4-1 and S4-2, Supporting Information). Figure 4b shows the cumulative probability of the resistance at V_{READ} and V_{READ}/2 in the 1S1R device. Since the RRAM and the selection device exhibited stable memory operation and highly nonlinear performance, respectively, a negligible degradation of resistance in the 1S1R device was observed up to 100 dc cycles. Furthermore, stable retention was also confirmed at 85 °C for 10^4 s as shown in Figure 4c. On the basis of the above results, we can suggest the Pt/TaO_x/TiO_2/TaO_x/Pt stack has a great potential for use in the selection device for suppressing the sneak current in the cross-point array. Compared to other reported selection devices (see Figure S5, Supporting Information), our device exhibited not only a high current density but also a high nonlinearity, which is a crucial component for suppressing the leakage current of RRAM and achieving high-density memory arrays.

CONCLUSION

In conclusion, we have proposed a high-performance selection device by utilizing the concept of a crested oxide barrier for high-density bipolar resistive memory applications. Owing to the Ta incorporation, the crested oxide barrier was formed in the TiO_2 layer, and thereby, the high current density of more than 10^7 A cm^{-2} and excellent nonlinear characteristics up to 10^4 were successfully demonstrated. Furthermore, the 1S1R device confirmed

the significant suppression of the leakage current compared to the RRAM device. These results strongly suggest that the selection device based on the $TaO_x/TiO_2/TaO_x$ structure opens up great opportunities to realize ultra-high-density bipolar RRAM arrays.

EXPERIMENTAL METHODS

First, a 100-nm-thick Pt bottom electrode was deposited by direct (dc) sputtering on a $TiN/SiO_2/Si$ substrate. For the isolation layer, 100-nm-thick SiO_2 was deposited on the Pt bottom electrode by plasma-enhanced chemical vapor deposition, and conventional lithography was used to define 250-nm *via* holes followed by reactive ion etching. After that, 10-nm-thick Ta was deposited by dc sputtering and annealed at 300 °C in a furnace tube for 30 min under ambient O_2. Subsequently, 4-nm-thick TiO_2 was deposited by ALD at 150 °C using titanium tetra-isopropoxide as the precursor and H_2O as the oxidizer. Then, 10-nm-thick Ta was again deposited by dc sputtering and annealed at 300 °C in the furnace tube for 30 min under ambient O_2. Finally, the 100-nm-thick Pt top electrode was defined by dc sputtering by shadow masking.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Requirements for selection device in the cross-point array; AES depth profile of $Pt/TiO_2/Pt$, $Pt/TaO_x/Pt$, and $Pt/TaO_x/TiO_2/TaO_x/Pt$ stacks; electrical properties of $Pt/Cu{:}HfO_2/Pt$ device used for 1S1R configuration; operation principle of 1S1R device; calculation of readout margin in the cross-point array; and comparison of selection device performances. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. *International Technology Roadmap for Semiconductor (ITRS)*, ITRS, 2011, http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ERD.pdf.
2. Waser, R.; Aono, M. Nanoionics-Based Resistive Switching Memories. *Nat. Mater.* **2007**, *6*, 833–840.
3. Sawa, A. Resistive Switching in Transition Metal Oxides. *Mater. Today* **2008**, *11*, 28–36.
4. Hasegawa, Tsuyoshi; Terabe, K.; Tsuruoka, T.; Aono, M. Atomic Switch: Atom/Ion Movement Controlled Devices for Beyond Von-Neumann Computers. *Adv. Mater.* **2012**, *24*, 252–267.
5. Lee, M.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y; Kim, C.; Seo, D. H.; Seo, S.; *et al.* A Fast, High-Endurance and Scalable Non-Volatile Memory Device Made from Asymmetric Ta_2O_{5-x}/TaO_{2-x} Bilayer Structures. *Nat. Mater.* **2011**, *10*, 625–630.
6. Ahn, S.; Lee, M.; Park, Y.; Kang, B. S.; Lee, C. B.; Kim, K. H.; Seo, S.; Suh, D.; Kim, D.; Hur, J.; *et al.* Write Current Reduction in Transition Metal Oxide Based Resistive-Change Memory. *Adv. Mater.* **2008**, *20*, 924–928.
7. Yang, J. J.; Zhang, M. X.; Strachan, J. P.; Miao, F.; Pickett, M. D.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. High Switching Endurance in TaO_x Memristive Devices. *Appl. Phys. Lett.* **2010**, *97*, 232102.
8. Tsubouchi, K.; Ohkubo, I.; Kumigashira, H.; Ochima, M.; Matsumoto, Y.; Itaka, K.; Ohnishi, T.; Lippmaa, M.; Koinuma, H. High-Throughput Characterization of Metal Electrode Performance for Electric-Field-Induced Resistive Switching in $Metal/Pr_{0.7}Ca_{0.3}MnO_3/Metal$ Structures. *Adv. Mater.* **2007**, *19*, 1711–1713.
9. Cario, L.; Vaju, C.; Corraze, B.; Guiot, V.; Janod, E. Electric-Field-Induced Resistive Switching in a Family of Mott Insulators: Towards a New Class of RRAM Memories. *Adv. Mater.* **2010**, *22*, 5193–5197.
10. Cheng, C.; Yeh, F.; Chin, A. Low-Power High-Performance Non-Volatile Memory on a Flexible Substrate with Excellent Endurance. *Adv. Mater.* **2011**, *23*, 902–905.
11. Chen, L.; Xu, Y.; Sun, Q.; Zhou, P.; Wang, P.; Ding, S.; Zhang, D. W. Atomic-Layer-Deposited HfLaO-Based Resistive Switching Memories with Superior Performance. *IEEE Electron Device Lett.* **2010**, *31*, 1296–1298.
12. Miao, F.; Strachan, J. P.; Yang, J. J.; Zhang, M.; Goldfarb, I.; Torrezan, A. C.; Eschbach, P.; Kelly, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-Performance Memristor. *Adv. Mater.* **2011**, *23*, 5633–5640.
13. Kawai, M.; Ito, K.; Ichikawa, N.; Shimakawa, Y. Thermally Formed Conducting Filaments in a Single-Crystalline NiO Thin Film. *Appl. Phys. Lett.* **2010**, *96*, 072106.
14. Yan, Z. B.; Li, S. Z.; Wang, K. F.; Liu, J.-M. Unipolar Resistive Switching Effect in $YMn_{1-x}O_3$ Thin Films. *Appl. Phys. Lett.* **2010**, *96*, 012103.
15. Wang, Y.; Liu, Q.; Long, S.; Wang, W.; Wang, Q.; Zhang, M.; Zhang, S.; Li, Y.; Zuo, Q.; Yang, J.; *et al.* Investigation of Resistive Switching in Cu-Doped HfO_2 Thin Film for Multilevel Non-Volatile Memory Applications. *Nanotechnology* **2010**, *21*, 045202.
16. Yan, Z.; Guo, Y.; Zhang, G.; Liu, J. −M. High-Performance Programmable Memory Devices Based on Co-Doped $BaTiO_3$. *Adv. Mater.* **2011**, *23*, 1351–1355.
17. Lian, W.; Lv, H.; Liu, Q.; Long, S.; Wang, W.; Wang, Y.; Li, Y.; Zhang, S.; Dai, Y.; Chen, J.; *et al.* Improved Resistive Switching Uniformity in $Cu/HfO_2/Pt$ Devices by Using Current Sweeping Mode. *IEEE Electron Device Lett.* **2011**, *32*, 1052–1054.
18. Linn, E.; Rosezin, R.; Kugeler, C.; Waser, R. Complementary Resistive Switches for Passive Nanocrossbar Memories. *Nat. Mater.* **2010**, *9*, 403–406.
19. Chang, S. H.; Lee, S. B.; Jeon, D. Y.; Park, S. J.; Kim, G. T.; Yang, S. M.; Chae, S. C.; Yoo, H. K.; Kang, B. S.; Lee, M.; *et al.* Oxide Double-Layer Nanocrossbar for Ultrahigh-Density Bipolar Resistive Memory. *Adv. Mater.* **2011**, *23*, 4063–4067.
20. Sheu, S.; Chiang, P.; Lin, W.; Lee, H.; Chen, P.; Chen, Y.; Wu, T.; Chen, F. T.; Su, K.; Cheng, K.; *et al.* A 5ns Fast Write Multi-Level Non-Volatile 1 K Bits RRAM Memory with Advance Write Scheme. *Symp. VLSI Circuits* **2009**, 82–83.
21. Gopalakrishnana, K.; Schenoy, R. S.; Rettner, C. T.; Virwani, K.; Bethune, D. S.; Shelby, R. M.; Burr, G. W.; Kellock, A.; King, R. S.; Nguyen, K; *et al.* Highly-Scalable Novel Access Device Based on Mixed Ionic Electronic Conduction (MIEC) Materials for High Density Phase Change Memory (PCM) Arrays. *Symp. VLSI Technol.* **2010**, 205–206.
22. Kau, D.; Tang, S.; Karpov, I. V.; Dodge, R.; Klehn, B.; Kalb, J. A.; Strand, J.; Diaz, A.; Leung, N.; Wu, J.; *et al.* A Stackable Cross Point Phase Change Memory. *IEDM Tech. Dig.* **2009**, 617–620.
23. Son, M.; Lee, J.; Park, J.; Shin, J.; Choi, G.; Jung, S.; Lee, W.; Kim, S.; Park, S.; Hwang, H. Excellent Selector Characteristics of Nanoscale VO_2 for High-Density Bipolar ReRAM Applications. *IEEE Electron Device Lett.* **2011**, *32*, 1579–1581.
24. Huang, J.; Tseng, Y.; Luo, W.; Hsu, C.; Hou, T. One Selector-One Resistor (1S1R) Crossbar Array for High-Density Flexible Memory Applications. *IEDM Tech. Dig.* **2011**, 733–736.
25. Kim, M. J.; Baek, I. G.; Ha, Y. H.; Baik, S. J.; Kim, J. H.; Seong, D. J.; Kim, S. J.; Kwon, Y. H.; Lim, C. R.; Park, H. K.; *et al.* Low Power Operating Bipolar TMO ReRAM for Sub 10 nm Era. *IEDM Tech. Dig.* **2010**, 444–447.
26. Likharev, K. K. Layered Tunnel Barriers for Nonvolatile Memory Devices. *Appl. Phys. Lett.* **1998**, *73*, 2137.
27. Sasago, Y.; Kinoshita, M.; Morikawa, T.; Kurotsuchi, K.; Hanzawa, S.; Mine, T.; Shima, A.; Fujisaki, Y.; Kume, H.; Moriya, H.; *et al.* Cross-Point Phase Change Memory with

$4F^2$ Cell Size Driven by Low-Contact-Resistivity Poly-Si Diode. *Symp. VLSI Technol.* **2009**, 24–25.
28. Furubayashi, Y.; Hitosugi, T; Yamamoto, Y.; Inaba, K.; Kinoda, G.; Hirose, Y.; Shimada, T.; Hasegawa, T. A Transparent Metal: Nb-Doped Anatase TiO_2. *Appl. Phys. Lett.* **2005**, *86*, 252101.
29. Navale, S. C.; Murugan, A. V.; Rabi, V. Varistor Based on Ta-Doped TiO_2. *Ceram. Int.* **2007**, *33*, 301–303.
30. Lee, C. B.; Lee, D. S.; Benayad, A.; Lee, S. R.; Chang, M.; Lee, M.; Hur, J.; Kim, Y. B.; Kim, C. J.; Chung, U. Highly Uniform Switching of Tantalum Embedded Amorphous Oxide Using Self-Compliance Bipolar Resistive Switching. *IEEE Electron Device Lett.* **2011**, *32*, 399–401.
31. Park, J.; Jung, S.; Lee, W.; Kim, S.; Shin, J.; Lee, D.; Woo, J.; Hwang, H. Improved Switching Variability and Stability by Activating a Single Conductive Filament. *IEEE Electron Device Lett.* **2012**, *33*, 646–648.